REMARKS

Examiner Brophy is thanked for her examination of the subject Patent Application. The Specification and Claims have been carefully reviewed with respect to the cited prior art, the Claim has been amended and is considered to be in condition for Allowance.

Briefly, the Applicants wish to point that a important fact has been overlooked by all during the interpretation and examination of the instant invention. A significant (previously unmentioned) difference between the instant invention and the cited prior art is thoroughly discussed below.

The claim was written in a manner which did not capture the essence of the drawings and specification together to reflect the important difference from the prior art. This has been corrected.

Additionally, this application is for a structured device made by a method described in US Patent, 6,358,796 B1 issued to the Applicants.

Initial Presentation of Argument

Instant Specification

The Applicants feel it is instructive to again present their specification but with highlights to adequately emphasize the facts to support the argument that the instant invention differs from the cited prior art. The entire section of the preferred embodiment is reproduced for the purpose of showing the entire sequence of manufacturing steps that produced the claimed device.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now to the drawings, specifically to Figs. 3a-3e, and to Figs. 4a-4g, there is shown a **method of forming a split-gate flash memory having a shallow trench isolation without the "smiling" structure of conventional cells.** This makes possible further shrinking of the lateral dimensions of a memory cell in addition to the scaling of the vertical dimension of a shallow trench for ultra scale integration of semiconductor devices. The top views of the

disclosed structure are shown Figs. 3a-3e while Figs. 4a-4g show the various cross-sectional views of the corresponding structure.

Fig. 3a shows top view of a semiconductor substrate (200) where trenches (205) are to be formed. A cross-sectional view of a trench is shown in Fig. 4a. **First, a layer of gate oxide (210), better seen in the cross-sectional view, is formed over the substrate** by thermally growing the oxide at a temperature between about 800 to 1100 °c, and preferably to a thickness between about 70 to 110 angstroms (A).

Next, first polysilicon layer (220), later to be formed into a floating gate, is deposited over the gate oxide later. Polysilicon is formed through methods including but not limited to Low Pressure Chemical Vapor Deposition (LPCVD) methods, Chemical Vapor Deposition (CVD) methods and .physical Vapor Deposition (PVD) sputtering methods employing suitable silicon source materials, preferably formed through a LPCVD method employing silane SiH_4 as a silicon source material at a temperature range between about 500 to 650 °C. The preferred thickness of the first polysilicon layer (220) is between about 800 to 1500 A. **This is followed by the forming of pad oxide layer (230)** which is to cushion, as is known in the art of LOCOS (Local Oxidationl of Silicon), the transition of stresses between the polysilicon layer (220) and the nitride layer (240) to be deposited subsequently. Pad oxide layer may be formed by using chemical CVD SiO_2, but it is preferred that it be grown thermally at a temperature range between about 900 to 1100 °c, and to a thickness between about 100 to 250 A.

A first nitride layer (240) is then formed over pad oxide layer (230) by reacting dichlorosilane ($SiCl_2H_2$) with ammonia (NH_3) in an LPCVD preferably at a temperature between about 720 to 820°C. The active regions in the substrate are now defined with a photolithographic step. A first photoresist layer (not shown) is patterned to protect. all of the areas where active devices are to be formed. **First nitride layer (240) is then dry etched** using recipe comprising gases SF_6, 02, and HBr, and **the pad, oxide layer is etched** by means of either a dry -or wet- etch. <u>**This is followed by forming a shallow trench in the silicon substrate**</u> by using a recipe comprising gases Cl_2 and HBr as shown in Fig. 4a. After forming the trench, **first photoresist layer is removed** by oxygen plasma ashing.

At the next step, and as a main, feature and key aspect of the present invention, trench (205) is lined with two thin conformal layers. First conformal layer comprises oxide and is thermally grown to a thickness of between about 200 to 550 A at a temperature range between about 850 to 1000°C. The second conformal layer comprises nitride and has only a thickness between about 100 to 300 A. <u>It will be appreciated by those skilled in the art that, at a later step of oxidizing the first polysilicon layer to form the floating gate of the memory cell, the presence of the second conformal nitride layer in the trench will prevent the oxidizing species from reaching the polysilicon surface to cause "smiling" effect as was shown in Fig. 1c.</u> This is because oxygen and water vapor diffuse very slowly through silicon nitride and nitride itself oxidizes very slowly. <u>***In a first embodiment of this invention, the nitride layer remains as an integral part of the structure as shown in Fig. 4a. In the second embodiment, the conformal nitride layer is etched to form nitride spacers (not shown).***</u>

With the two conformal layers lining the interior walls therefore, **isolation oxide is next deposited into trench (205)** using chemical vapor deposition to a thickness between about 4000 to 6000 A. As another key step, first

nitride layer (240) is removed by dry etching with gas SF6 and so is the pad oxide layer (230). Subsequently, a second blanket nitride layer (260) is deposited as- shown in Fig. 4b by reacting dichlorosilane ($SiCl_2H_2$) with ammonia (NH_3) in an LPCVD preferably at a temperature between about 750 to 850 °C. Fig. 4b is a cross section of the substrate shown in Fig. 3b. Then, a second photoresist layer, (270), is next formed and patterned to define the floating gate regions over the substrate as shown in Fig. 3c. The pattern openings, (275), are dry etched into the second nitride layer until the underlying polysilicon layer (220) is exposed. First polysilicon layer (220) is better seen in Fig. 4c. The exposed first polysilicon layer in the floating gate pattern openings in the second nitride layer are next oxidized in a wet environment and at a temperature between about 850 to 1000 °c to form poly-oxide "tops" (225) shown in Fig. 4c, with a preferred thickness between about ,1000 to 1800 A. <u>It is important to note here that, as a result of the main feature of having conformal layers (225) and (250) in trench (205), the "smiling" effect that would have otherwise been present has been eliminated. In other words, the oxidizing species have been prevented from reaching the polysilicon and forming the "smiling" structure.</u> Top view of the oxidized tops (225) of the first polysilicon layer are shown in Fig. 3d, and a cross-section of the same in Fig. 4d. Another view of trench (205)' is shown in Fig. 4e.

After the poly oxidation, second nitride layer (260) is removed by applying a wet solution of phosphoric acid, H_3PO_4. Using the poly-oxide layer as a hard mask, the first polysilicon layer is etched using a recipe comprising HBr, Cl_2 gases thus forming polysilicon floating gate (223) as shown in Fig. 3d.

The penultimate step of completing the forming of the split-gate memory cell structure is accomplished first by forming an inter-poly oxide (280) as shown in Fig. 4f. It is preferred that layer (280) is an oxide with a thickness between about 100 to 250 A. At the final step, a second polysilicon layer is deposited over inter-poly oxide (280) and is patterned with a third photoresist layer (290) shown in Fig. 3e, to form control gate (293), as shown in Fig. 4f.

It is preferred that the second polysilicon layer is formed using silicon source SiH_4 in an LPCVD chamber at a temperature between about 500 to 650 °c, and that it has a thickness between about 1000 to 3000 A. A cross-sectional view of shallow trench isolation (205) after the completion of the split-gate memory cell is shown in Fig. 4g.
<u>It has been disclosed in the present invention a split-gate flash memory cell having a shallow trench with a "non-smiling" structure and a method directed to forming the same.</u> Though numerous details of the disclosed method are set forth here, such as forming two conformal layers lining the interior walls of the trench, to provide an understanding of the present invention, it will be obvious, however, to those skilled in the art that these specific details need not be employed to practice the present invention, such as, for example, the forming of spacers from the nitride lining. At the same time, it will be evident that the same methods may be employed in other similar process steps, such as, .for example, in shrinking cell size further by preventing the formation of the "smiling" structure at the edge of floating gates of prior art.

That is to say, while the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

Note that the trenches in the instant invention are formed **after** the deposition of the gate oxide and the floating gate polysilicon. This is important.

Prior Art Ning et al.

The claim of prior art Ning et al is presented with respect to the process step sequence of forming trenches. These claims contain sequence information whereas the specification does not.

> Having thus described our invention, what we claim as new and desire to secure by Letters Patent is:
>
> 1. A method for fabricating a semiconductor memory cell comprising the steps of:
>
> **Step 1. forming isolation trenches in a silicon substrate,**
>
> Step 2. implanting first type dopants into the channel region of said substrate surface between said isolation trenches with a relatively low dosage,
>
> Step 3. masking a portion of said channel region of said substrate surface between said isolation trenches,
>
> Step 4. implanting second type dopants into the unmasked portions of said channel region of said substrate surface with a relatively high dosage, to provide a channel region having a low doped region and a high doped region,
>
> **Step 5. removing said mask from over said channel region and forming a floating gate element on said substrate surface over said low doped and high doped channel regions,**
>
> Step 6. forming a control gate region over said floating gate region.

Note that the trenches are formed **before** the formation of the floating gate. This is important.

Prior Art Hunter et al.

Also presented are the claims and specifications of prior art Hunter et al with respect to the sequence of steps of forming trenches.

What is claimed is:

1. A method of forming an isolation trench in a semiconductor device, comprising the steps of:

forming a trench in a silicon body,

forming a layer of insulating material over the interior walls of said trench, said layer being sufficiently thin to prevent increase of stress within said trench,

forming an oxidation masking layer over said layer of insulating material,

removing said oxidation masking layer from predetermined portions of said silicon body,

filling the remainder of said trench with a body of oxidizable isolation material, and then

oxidizing said silicon body to form a layer of field oxide over said predetermined portions of said semiconductor body and the filled trench while simultaneously oxidizing a surface portion of said isolation material, said oxidation masking layer preventing undesirable oxidation and stress within the semiconductor material which might otherwise cause dislocation defects.

2. The method of claim 1, wherein said oxidation masking layer comprises nitride.

3. The method of claim 1, wherein said layer of insulating material comprises silicon oxide.

4. The method of claim 1 wherein said isolation material filling the remaining area of said trench comprises polysilicon.

5. The method of claim 1, further comprising the steps of:

forming a second layer of insulating material over said oxidation masking layer, and

forming a second masking layer between said second layer and said body of isolation material.

6. The method of claim 1 wherein said layer of field oxide is formed at a temperature above 1000.degree. C.

7. The method of claim 1 wherein said oxidation masking layer has a thickness of from 300 .ANG. to 600 .ANG..

8. The method of claim 1 wherein said layer of insulating material has a thickness in the range of approximately 200 .ANG. to 450 .ANG..

The single nitride layer embodiment is found in the specification as follows:

FIG. 2 illustrates a trench construction which substantially eliminates the formation of defects or dislocations 30 and 32, as well as reducing the formation of the ***vertical bird's beak structure*** into the trench. **The trench shown in FIG. 2 is initially constructed by forming a trench 36 by etching or other conventional techniques.** For example, the etch mask pattern for the trench 36 may be defined in an **oxide layer** (for example, thermal or CVD oxide) **formed on the substrate surface, which is used as a hard mask for an etch** and a chlorine-based reactive-ion-etching process with a silicon-to-oxide etch ratio of about 15:1. Trench 36 has dimensions similar to previously developed trenches and may be provided with a depth of from about 3 to 10 microns, depending on epilayer thickness. The width of the trench may range from 0.5 micron to 2.5 microns, depending upon its intended use. **After removal of the hard mask, a relatively thin layer of oxide 38 is formed on the inside sidewalls and bottom of the trench 36, as well as over the upper face of regions 10 and 12.** The thickness of the oxide layer 38 may range, for example, from 200 .ANG. to 450 .ANG.. It has been found that by forming such a thin layer of oxide, the stresses which heretofore created the defects 30 tend to be eliminated.

A thin oxidation masking layer 40 of nitride is then formed over the entire oxide layer 38 by conventional LPCVD techniques. Oxidation masking layer 40 may have, for example, a thickness of from 300 .ANG. to 600 .ANG.. **The nitride layer protects the substrate and the subsequent**

> polysilicon refill from oxidation which is the cause of the vertical bird's beak 34a-b. The nitride layer 40 also tends to reduce electrical cross talk between the P well 10 and N well 12 because of its insulating properties.
>
> The trench 36 is then refilled with thick oxide or undoped polysilicon 42. If refilled with oxide, the upper portion of the oxide 42 is planarized to the silicon surface, the previously applied nitride on the surface of the substrate is stripped, and a thick field oxide layer 44 is grown. If refilled with polysilicon, then a cap oxide 43 may be grown either before field oxide layer 44, or simultaneously with the thick field oxide.

It matters not that the trench is filled with polysilicon or an oxide. It matters not that Hunter et al. require a doubling of the oxide/nitride layering in the case of filling the trench with polysilicon, which by the way, would really preclude Hunter et al. from being bon-a-fide rejection prior art, where the instant invention employs a single layer for both oxide and polysilicon fillers. Therefore viewing only the first embodiment (the single nitride layer) of Hunter et al. as resembling a portion of the instant invention, it is shown that the thin oxide/nitride layer is applied to the walls of the trench formed in a **bare** (no gate oxide or polysilicon gate layers present) silicon substrate covered with a hard mask of oxide. That hard mask is removed and a field oxide is then grown. Note, herein the trenches are also created **before** the field oxide (gate oxide) is formed. This again is important. Moreover, the specification makes no reference to a **gate** of any kind, let alone a **floating gate** of a memory cell.

DETAILED ACTION

Claim Rejections - 35 USC § 103

Reconsideration of the rejection of Claims 34 under 35 USC 103 (a) as being unpatentable over Ning et al (5,231,299) in view of Hunter et al. (4,631,803) is requested on the following arguments:

Applicants are in agreement with the Examiner that Ning et al. do not teach that there are two conformal layers lining the inside walls of the trench. The Applicants have previously pointed to the fact that Hunter et al. requires four thick (4) layers covering the trench if a polysilicon is used to fill the trench. However, the Applicants now point out the most significant differences to Ning et al. and Hunter et al with the following additional arguments based on the information presented above.

Significance of Sequence in Trench Formation

As highlighted above in the instant specification:

> Ina first embodiment of this invention, the **nitride layer remains as an integral part of the structure as shown in Fig. 4a.** In the second embodiment, the conformal nitride layer is etched to form nitride spacers (not shown).

Shown in Fig. 4a is nitride layer (250) vertically covering **not only** the substrate (200) and the gate oxide (210) **but also** the polysilicon (220), the pad oxide (230) and the first nitride (240). In this structure the gate oxide (210), the pad oxide (230) and the polysilicon (220) sandwiched in between are protected from subsequent oxidizing operations. No such protection of polysilicon (present or yet to be deposited) is available in either Ning et al. or Hunter et al.

One would not be motivated by the teachings of Ning et al. and Hunter et al., to consider an appropriate sequence of manufacturing steps to protect the polysilicon and its interfaces from oxidizing operations by use of a thin nitride film.

Ning et al. teaches a method of forming a memory cell having a selective channel implant to provide high speed channel hot electron programming from

the high doped channel region of the EEPROM cell while maintaining high read current from the low doped channel region. In doing so, Ning et al. merely introduces shallow trench isolation regions (12, 14) in proximity to a channel (16, 18 and 20).

Hunter et al. is then seemingly relied upon to teach how to make those shallow isolation trenches having conformal oxide and nitride layers. Hunter et al. is interested in preventing defects in the substrate and even precludes "vertical bird's beaks" as a byproduct of that effort.

But that is where the teaching ceases. Ning et al. would suffer the "smiling effect". And although Hunter et al. has addressed "vertical bird's beaks" in initial formation of trenches, they do not teach the later prevention of "smiling" polysilicon. Additionally, early "bird's beak" in trench polysilicon is only precluded by a thick double oxide/nitride layering.

The claim has been amended to express the instant invention, namely that the polysilicon gate layer is protected by the single thin conformal oxide/nitride layer set applied to the trench.

We have reviewed the related art references made of record and agree with the Examiner that none of these suggest the present claimed invention.

In light of the above arguments, it is suggested that the specification adequately describes the invention and that the Claims now clearly distinguish the invention from the prior art. All claims are therefore believed to be in condition for allowance.

Allowance of all claims is therefore respectfully requested.

It is request that should Examiner Mulpuri not find that the Claims are now Allowable that the Examiner call the undersigned attorney at 845-452-5863 to overcome any problems preventing allowance.

Respectfully submitted,

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MARKED UP COPY OF CLAIMS

34. (AMENDED TWICE) A split-gate flash memory having a non-smiling trench isolation comprising:

a substrate;

a first gate oxide layer atop the substrate;

a floating gate atop the gate oxide layer;

a trench formed through the floating gate and gate oxide layers into the substrate wherein the vertical surfaces of the floating gate, the gate oxide layer and the substrate form interior trench walls;

two conformal layers lining the [inside] interior trench walls [of said trench], wherein a first conformal layer [lining] comprises oxide having a thickness between about 200 to 550 Å, and a second conformal layer [lining] comprises nitride having a thickness between about 100 to 300 Å;

a second gate oxide; and

a control gate atop the second gate oxide.